SiPM Signal Acquisition System Based on a Sigma-Delta Modulator

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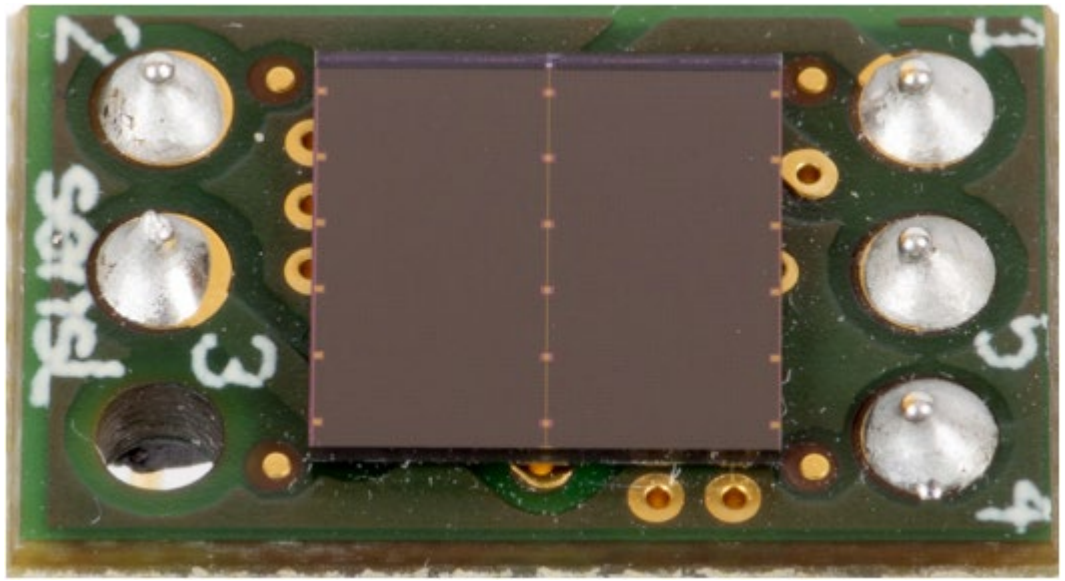
OUTLINE

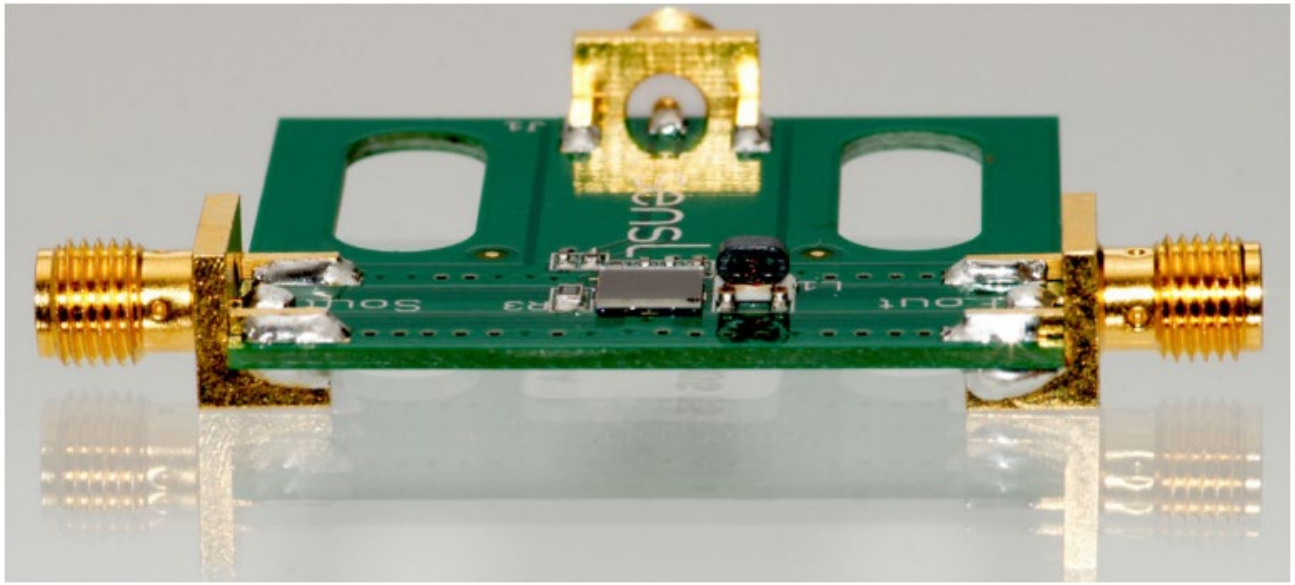
1. Introduction
2. System architecture and circuit implementation
3. Simulations
4. Measurements
5. Conclusions

SiPMs

SiPMs are a good alternative to traditional photomultiplier tubes due to:

1. Low operating voltage,
2. Robustness and compactness,
3. Low sensitivity to magnetic fields
4. Well suited for operation at cryogenic temperatures

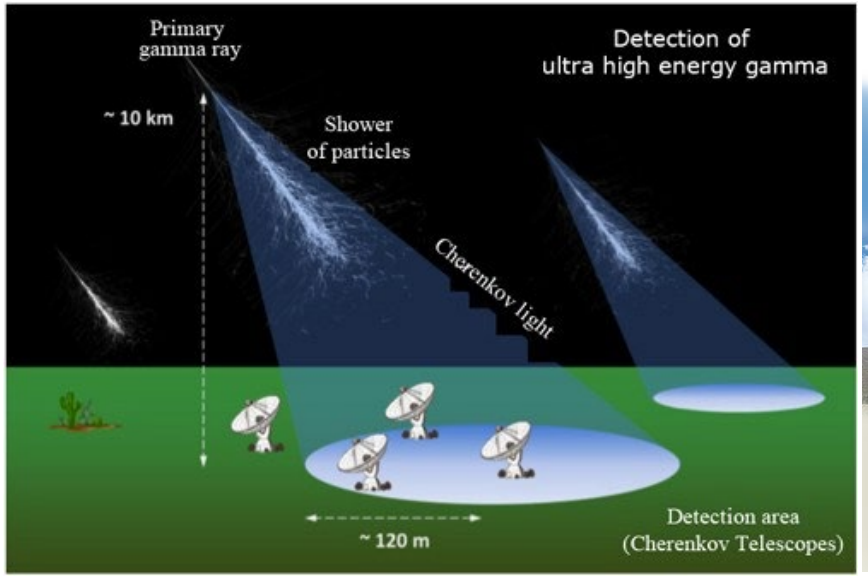


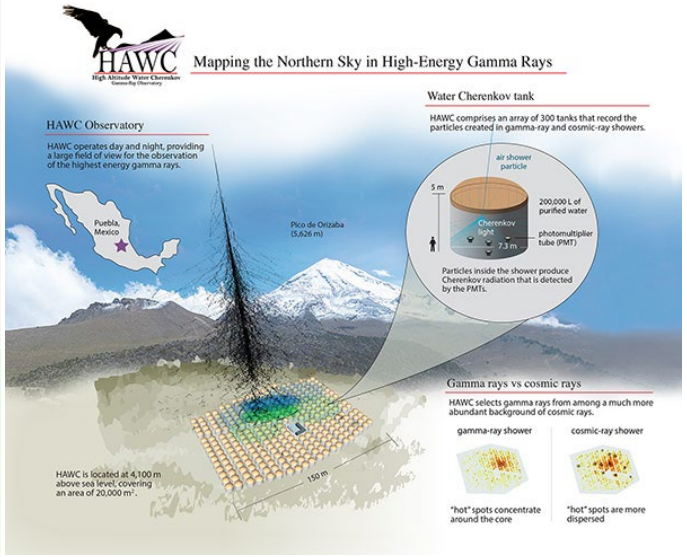


https://www.onsemi.com/pdf/datasheet/microj-series-d.pdf

SiPMs Applications

- Medical imaging
- Hazard and threat detection
- High energy gamma rays and Cherenkov light detection
- Ranging (LiDAR)





https://images.google.com/

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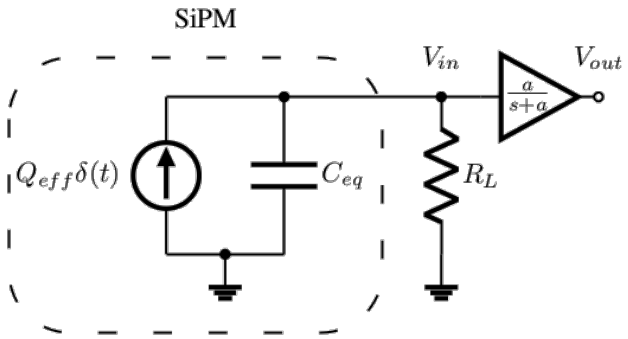
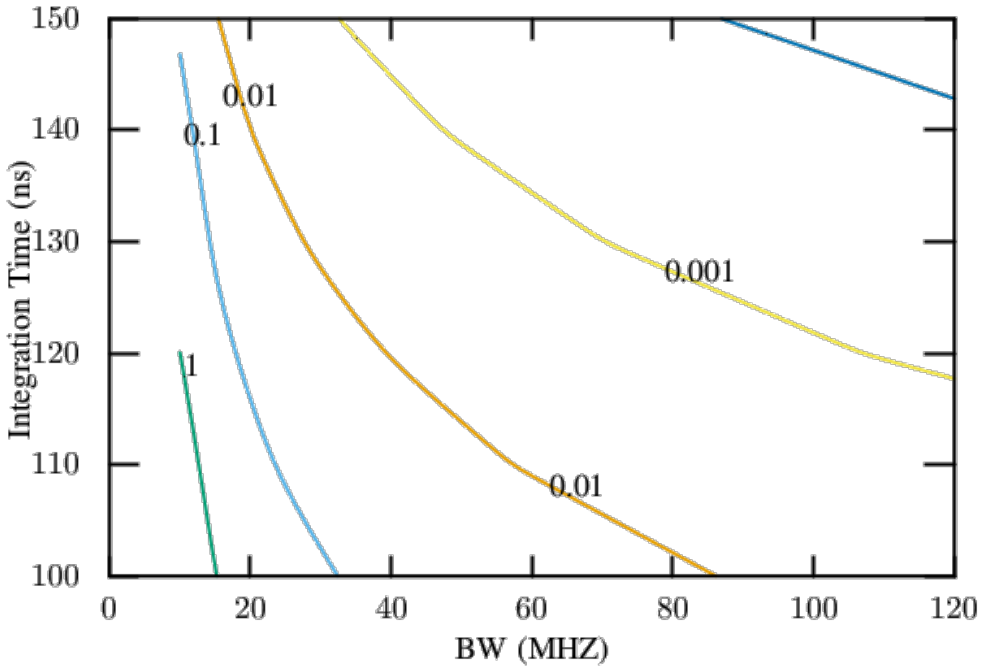
BANDWIDTH REQUIREMENTS

Importance of Bandwidth (BW):

- The SiPM's bandwidth is critical as it sets the minimum bandwidth for the input amplifier and subsequent stages.
- A reduced bandwidth may result in information loss, while a wider bandwidth can introduce more noise to the signal of interest.

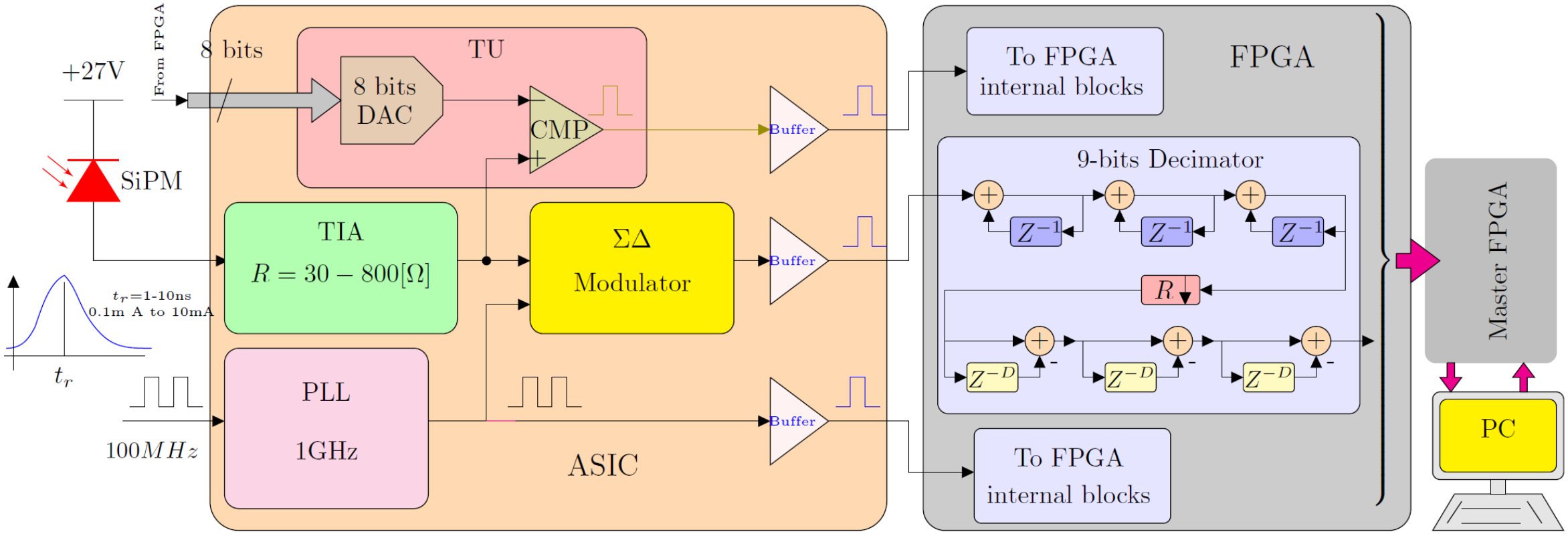




Amplifier Bandwidth Error Model:
We use a circuit with a SiPM model, an RL resistor converting SiPM current to voltage, and a one-pole voltage buffer to represent the amplifier's bandwidth.

- Contour-line graph illustrates the relative error as a function of BW and integration time constant.
- A 10 MHz BW achieves 99% precision, allowing for a reduction in bandwidth in the Sigma-Delta Modulator without significant information loss.

SYSTEM ARCHITECTURE

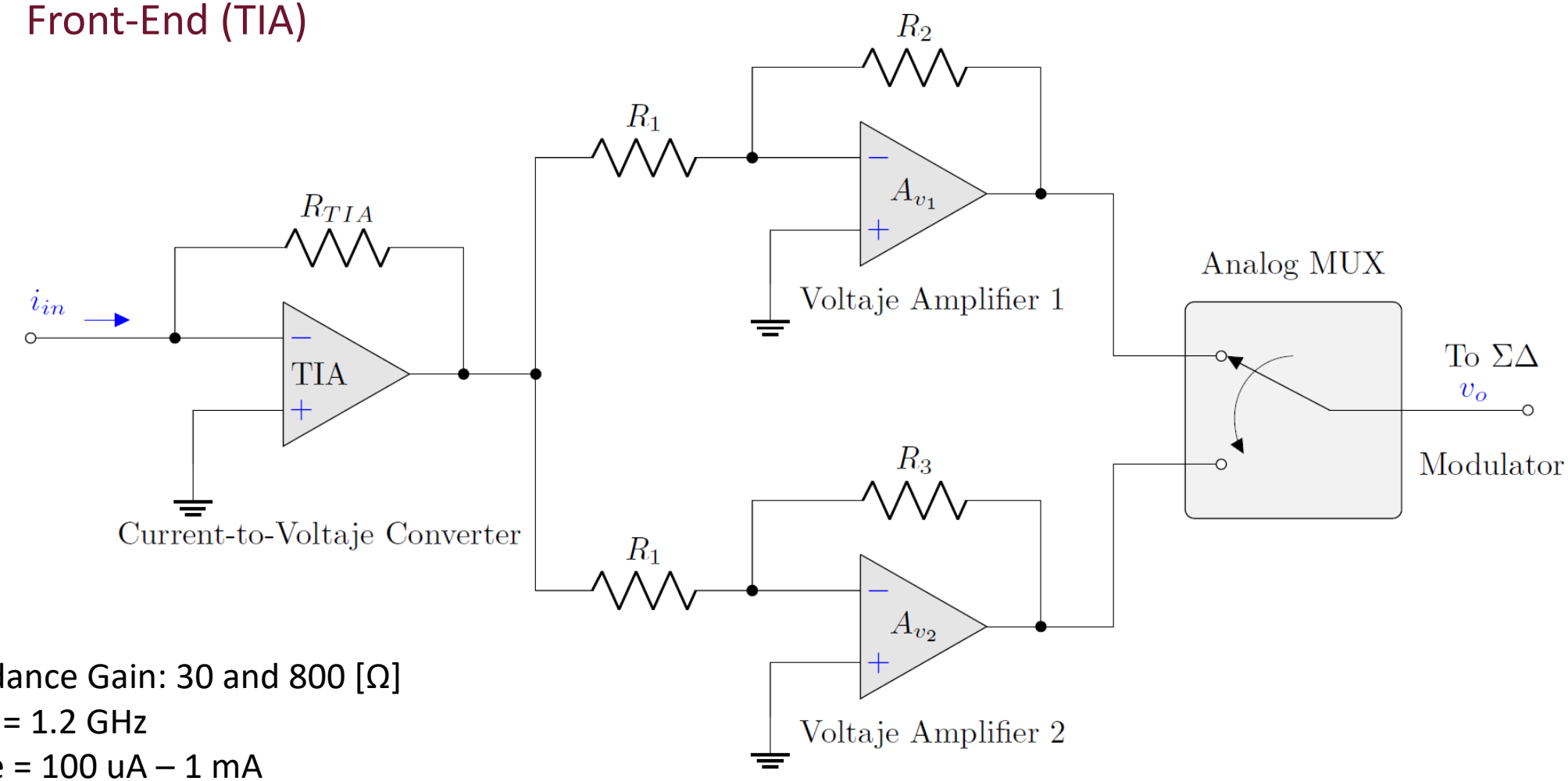


- Transimpedance Gain: 30 and 800 [Ω]
- Bandwidth= 10 MHz
- Input range = 100 uA – 1 mA
- Voltage Supply= ± 0.9 V
- Current consumption = 290 mA*
- ENOB = 5.49 bits (measured)
- 180 nm CMOS standard

* Includes I/O buffers, PLL, and analog biasing circuitry.

SYSTEM IMPLEMENTATION

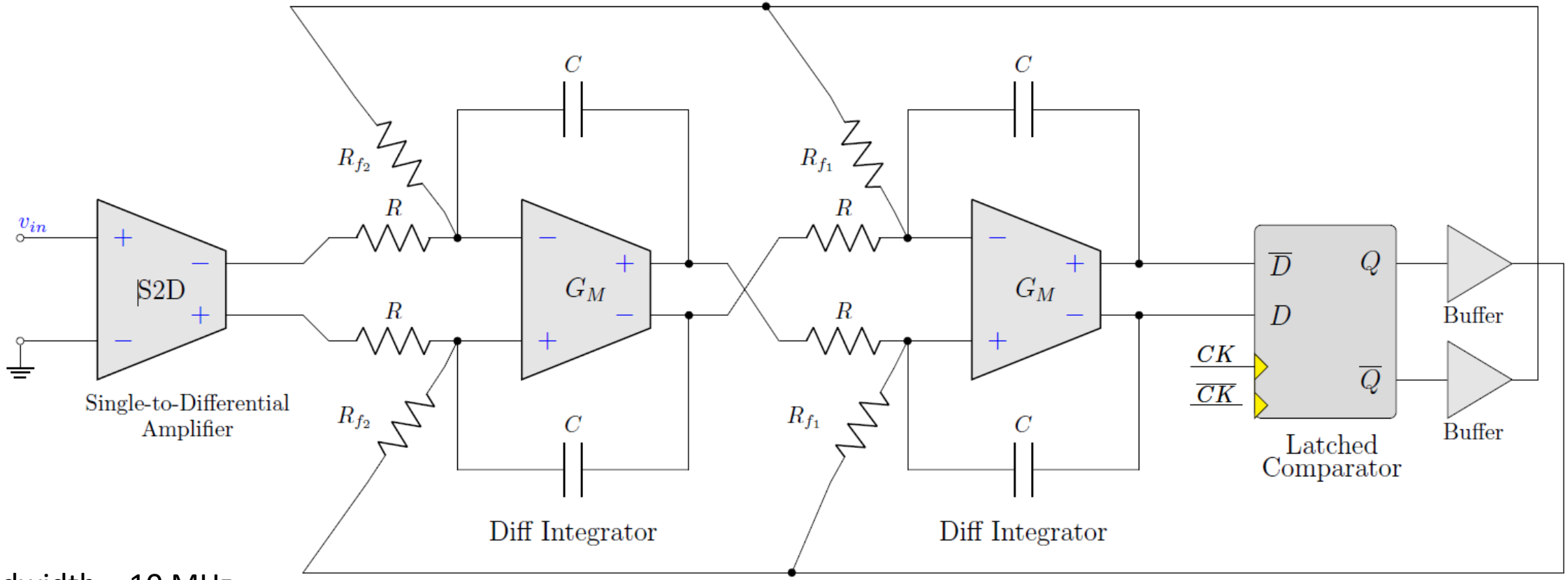
Front-End (TIA)



- Transimpedance Gain: 30 and 800 [Ω]
- Bandwidth = 1.2 GHz
- Input range = 100 uA – 1 mA
- Voltage Supply= ±0.9V
- Current consumption = 54.3 mA

SYSTEM IMPLEMENTATION

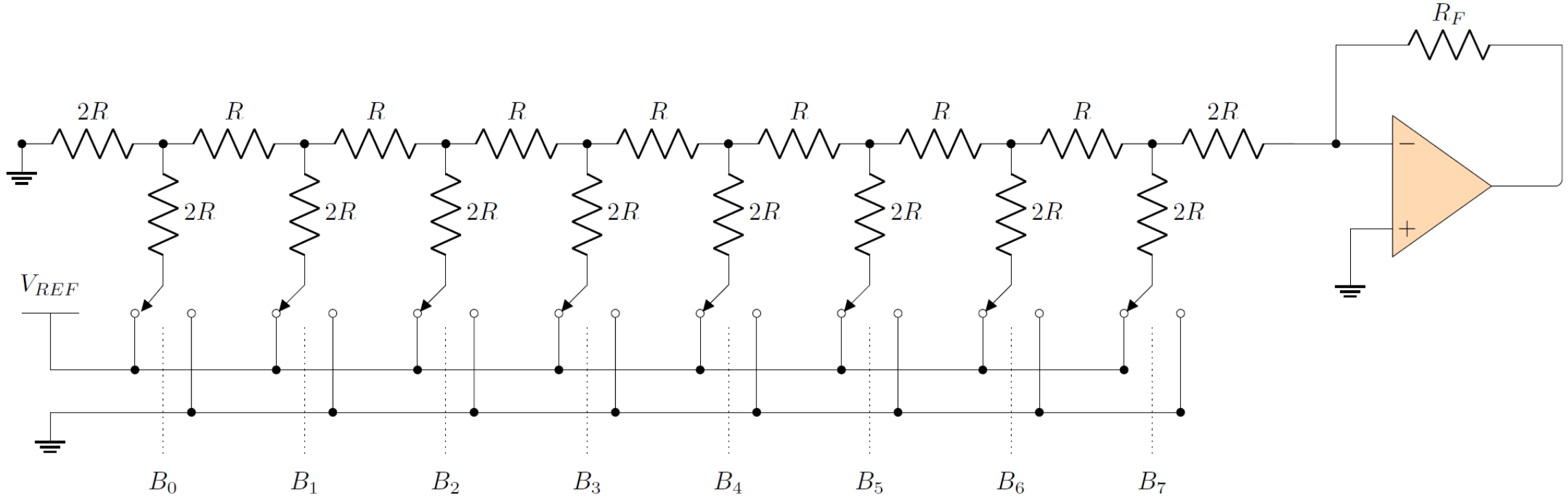
2nd order ∑Δ Modulator



- Bandwidth = 10 MHz
- OSR = 50
- Input range = -0.45 V to 0.45 V
- Voltage Supply = ±0.9 V
- Current consumption = 180 mA

SYSTEM IMPLEMENTATION

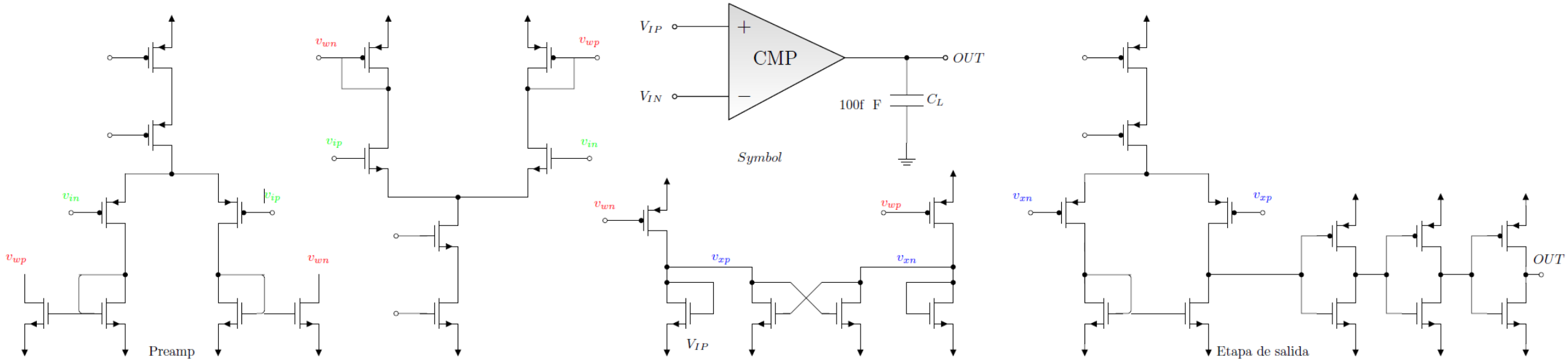
Trigger Unit
8-bit Digital to Analog Converter



- R-2R architecture.
- Vref ± = ± 0.65
- Resolution = 8 bits.
- OTA = 45 dB Gain, 10 MHz GBW
- Voltage Supply= ±0.9 V
- Current consumption = 1.5 mA

SYSTEM IMPLEMENTATION

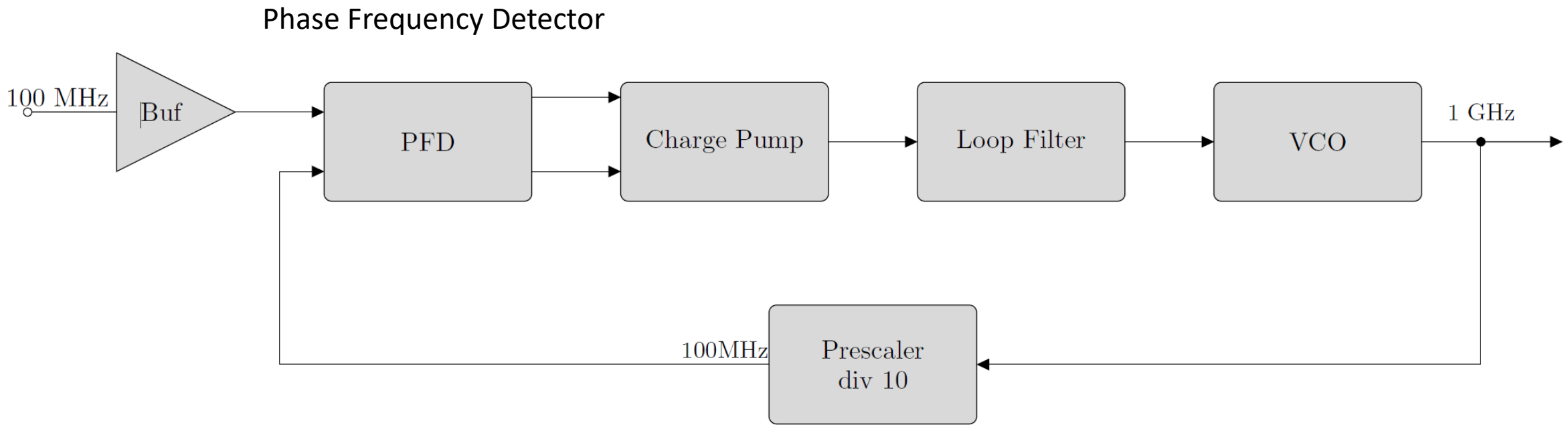
Trigger Unit
Comparator



- Rail-to-Rail input.
- Min comparation level = 5 mV
- Rising and falling time = 100 ps
- Voltage Supply= ±0.9 V
- Current consumption = 10 mA

SYSTEM IMPLEMENTATION

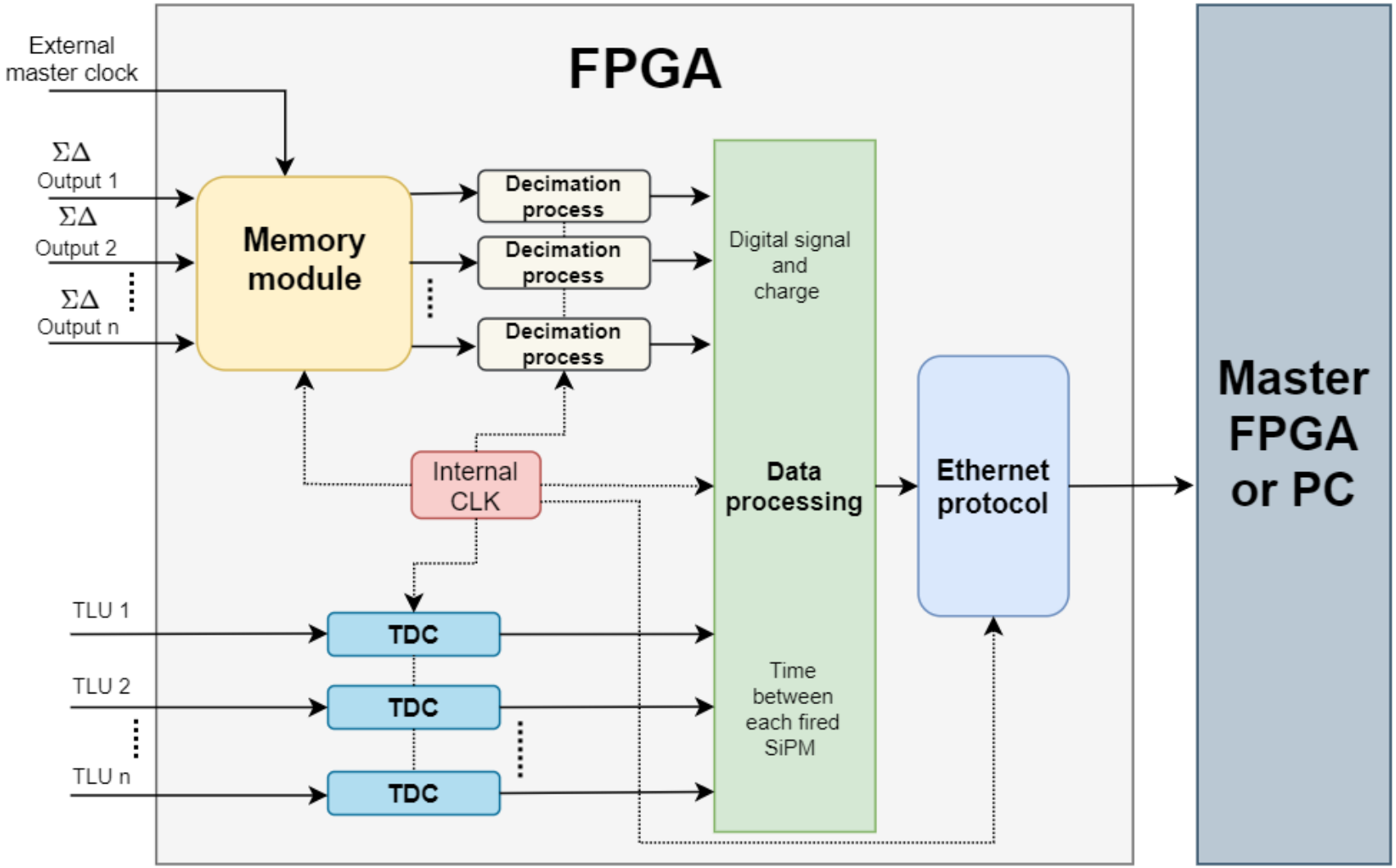
Classical PLL Configuration



- Classic analog PLL.
- Clock reference =100 MHz
- Clock output = 1 GHz
- LC tank VCO.
- Voltage Supply= ±0.9V
- Current consumption = 22 mA

SYSTEM IMPLEMENTATION

FPGA Post-Processing Unit



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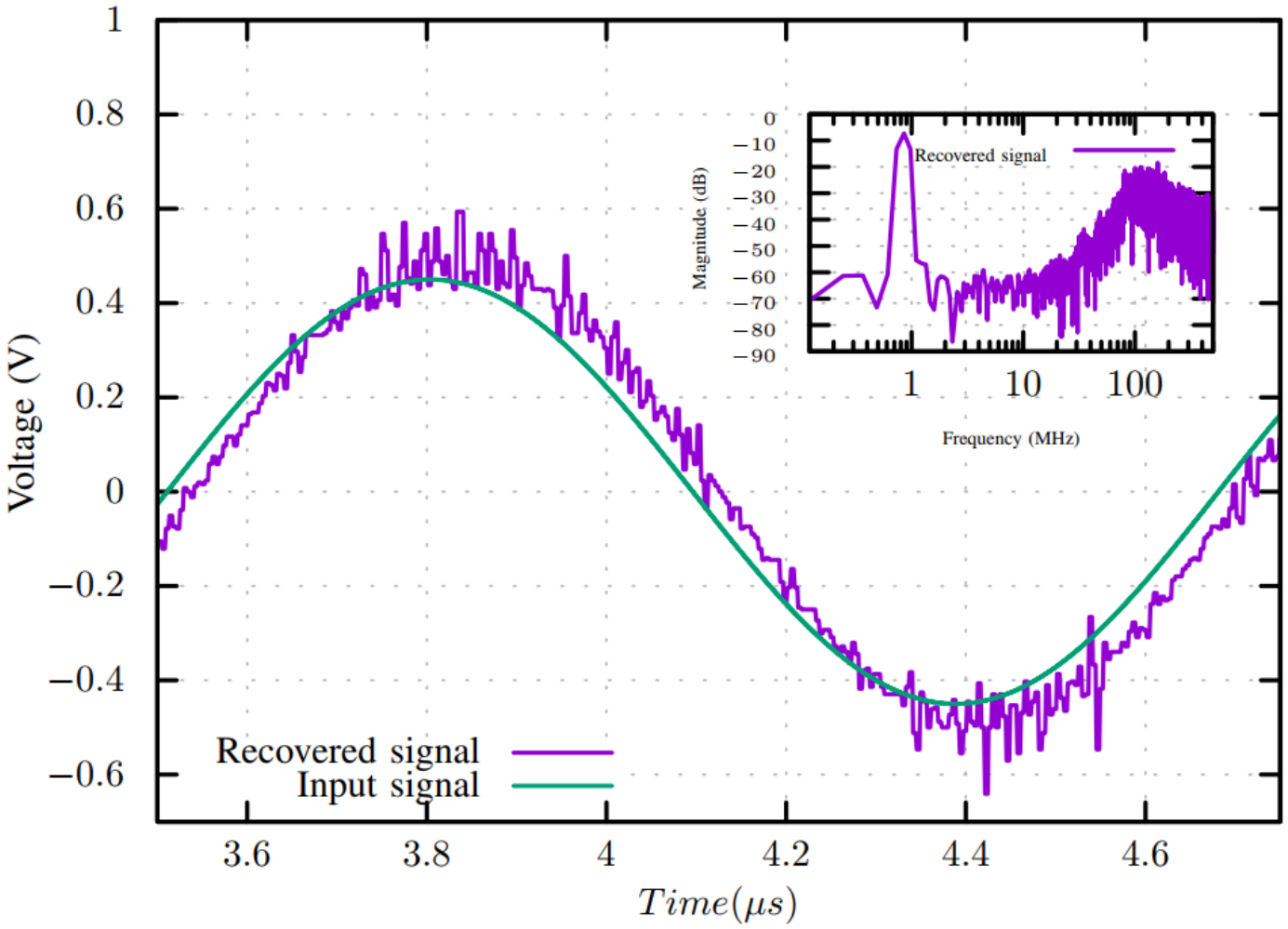
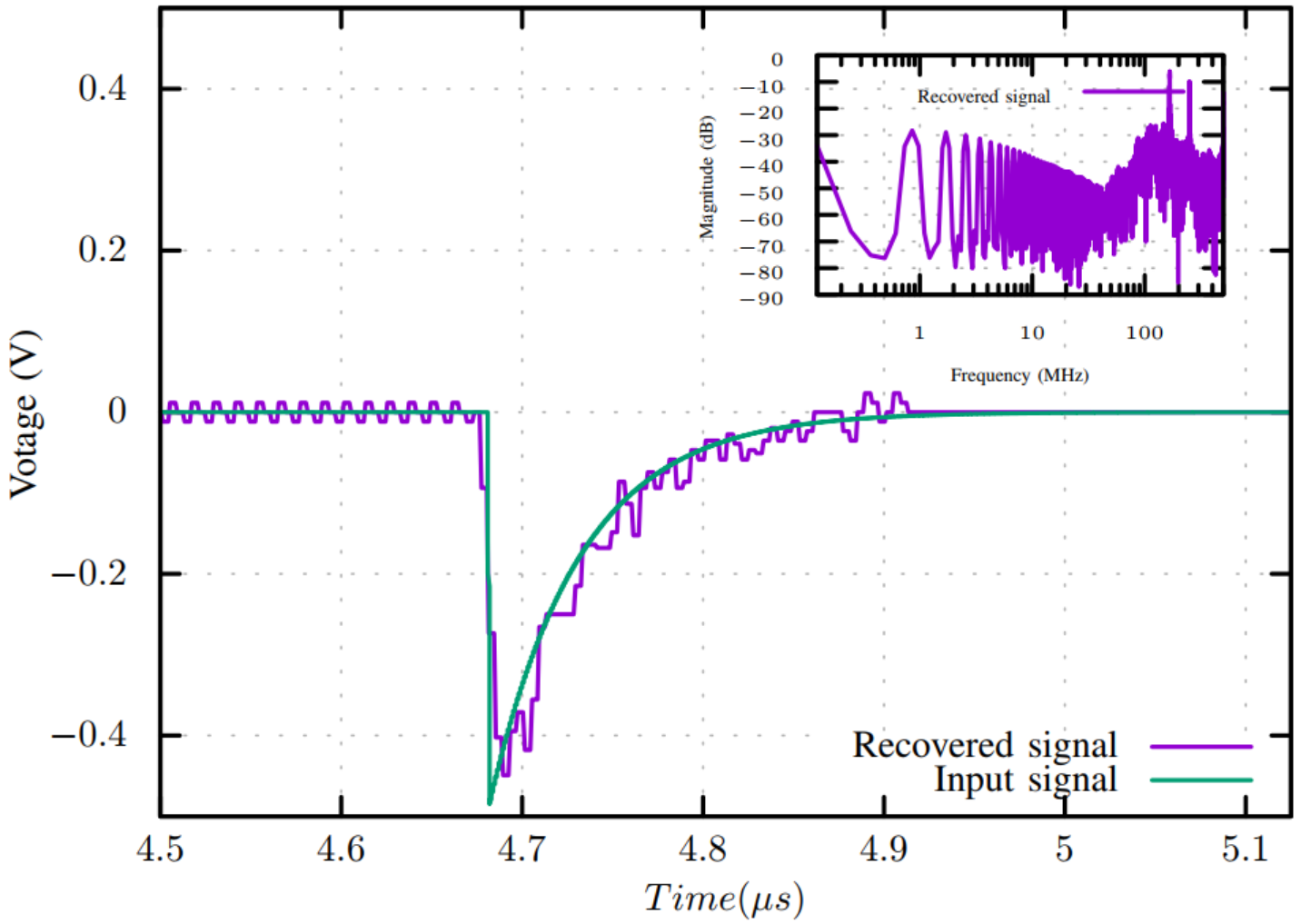
SIMULATIONS: Sinusoidal.



Post-layout simulations.

- Sine wave input = 0.45 V @ 854.4 kHz
- Sampling frequency = 1 GHz
- ENOB = 6.4 Bits

SIMULATIONS: SiPM.



Post-layout simulations.

- SiPM pulse input
  - * Amplitude: 0.45 V
  - * Peak-time: 5ns
  - * Discharge phase: 200 ns

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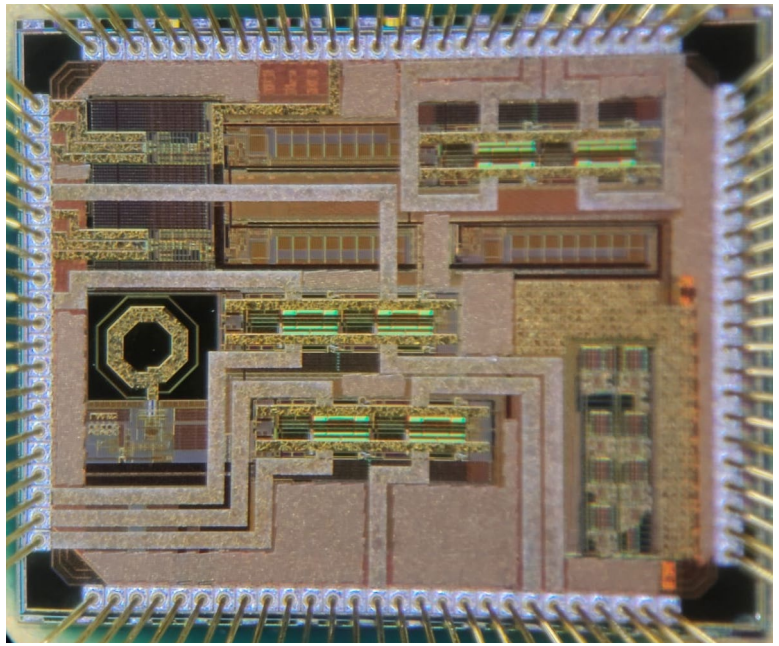
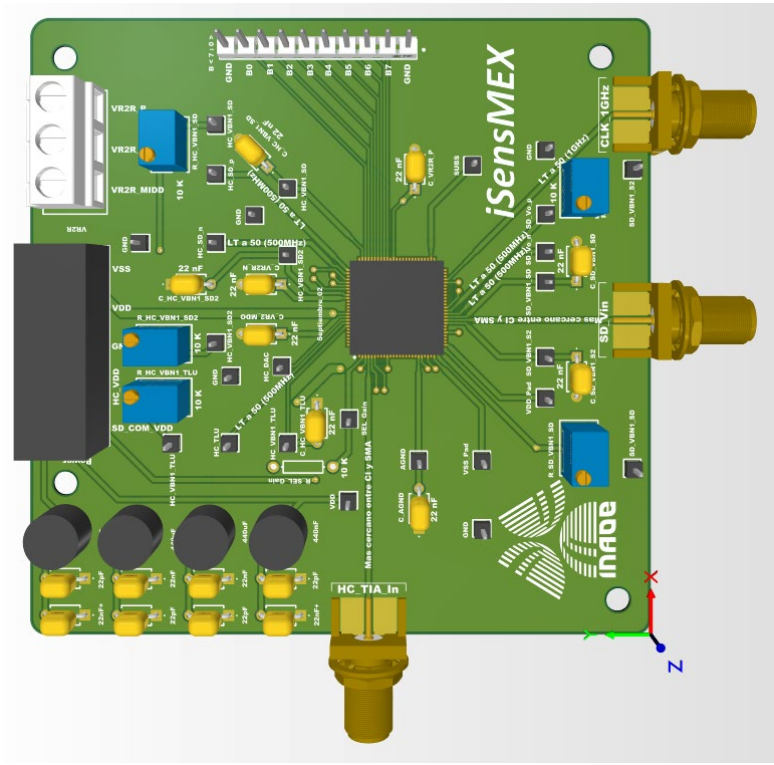
MEASUREMENTS

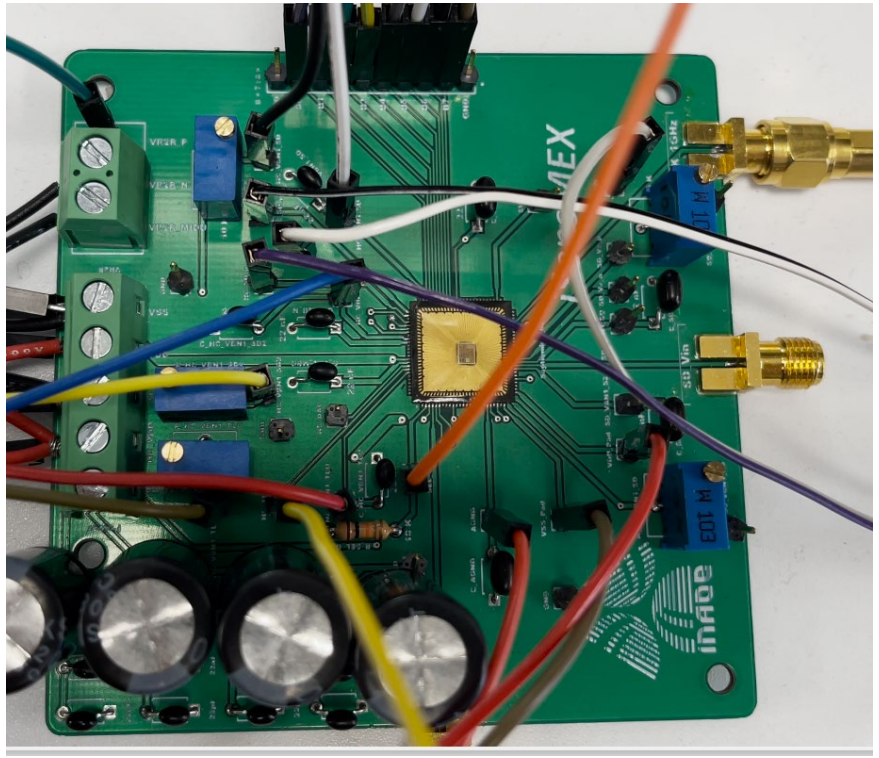
PCB



2mm x 2.5mm die
QFN-100 package



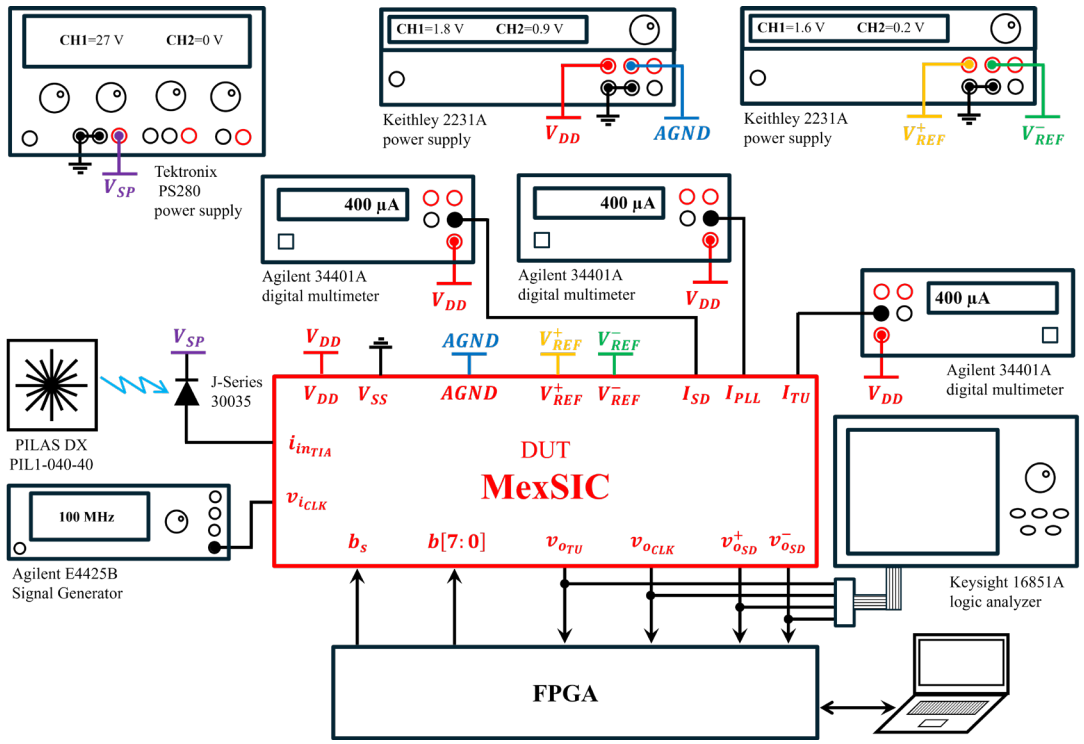
3D- MODEL
FR4 PCB

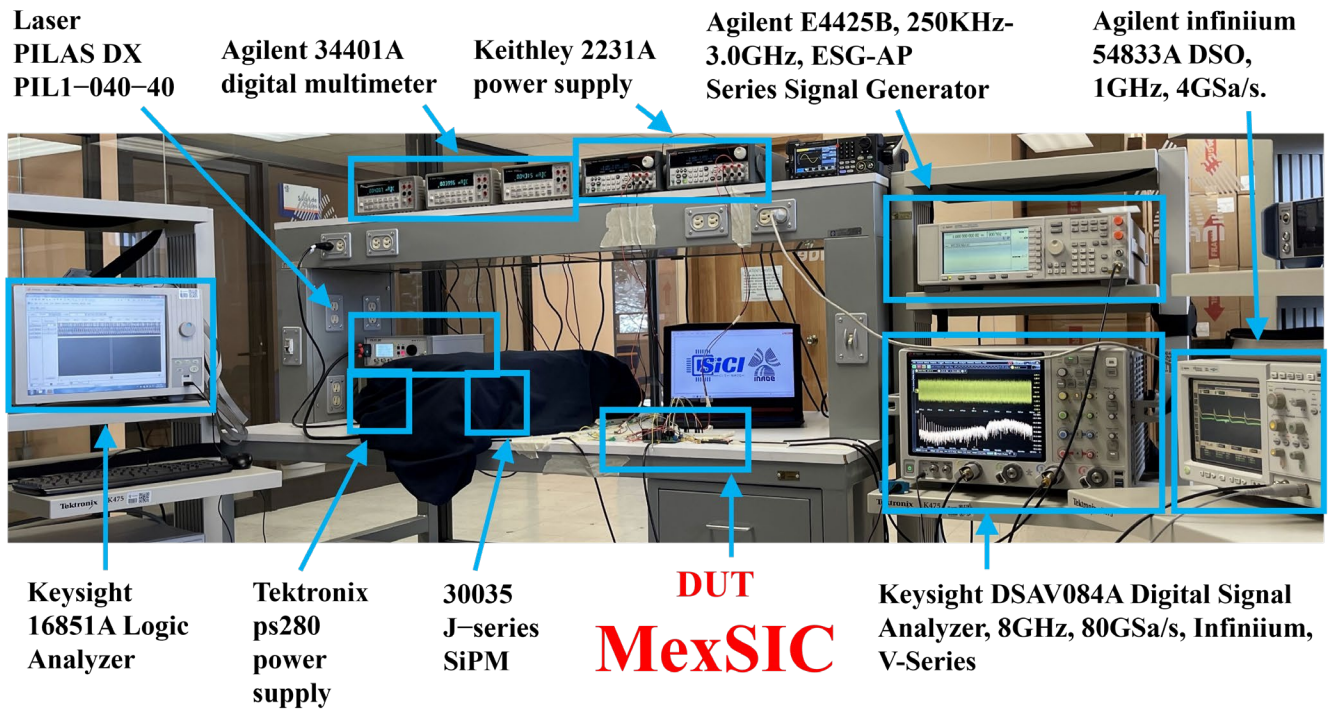


Chip + PCB assembly

MEASUREMENTS

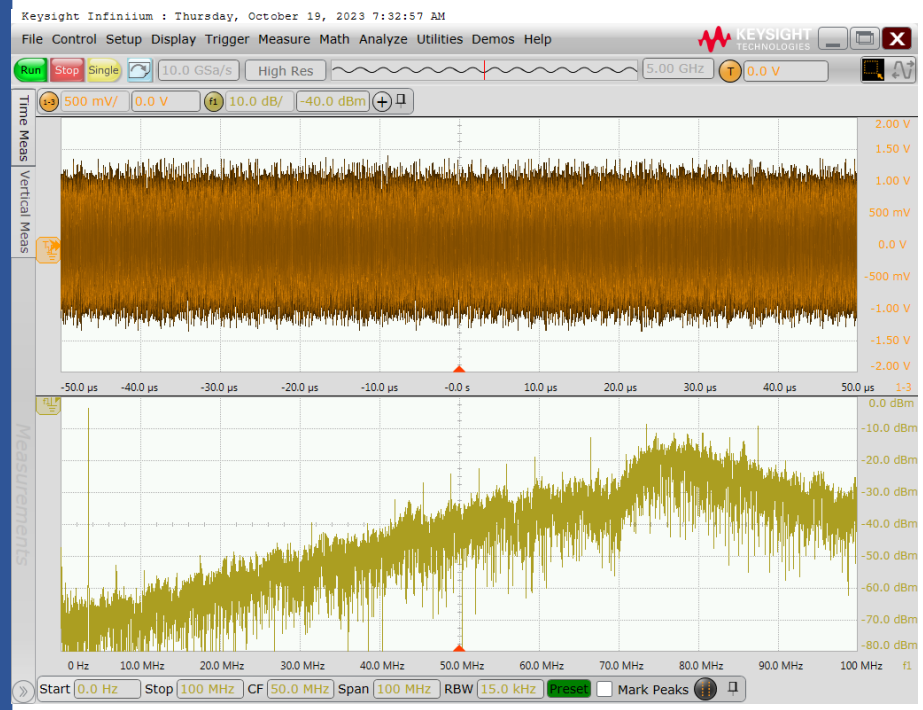
Test-bench

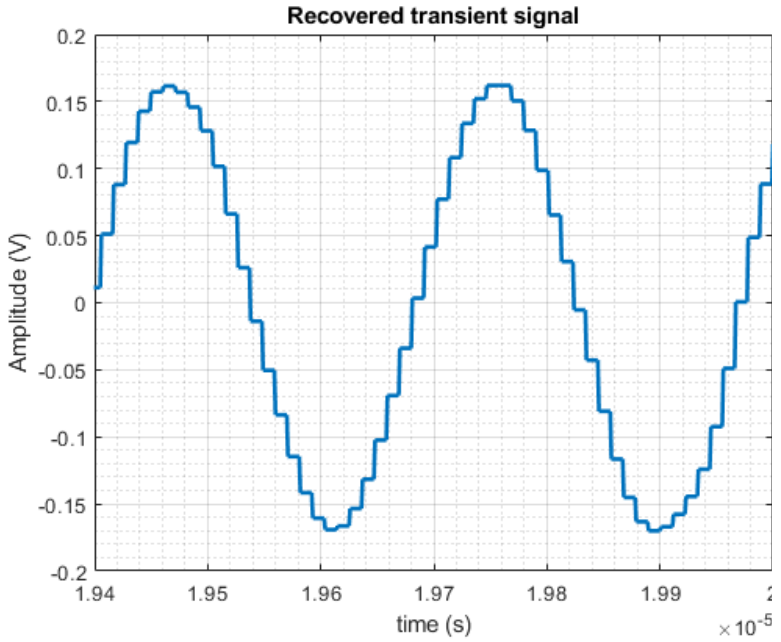


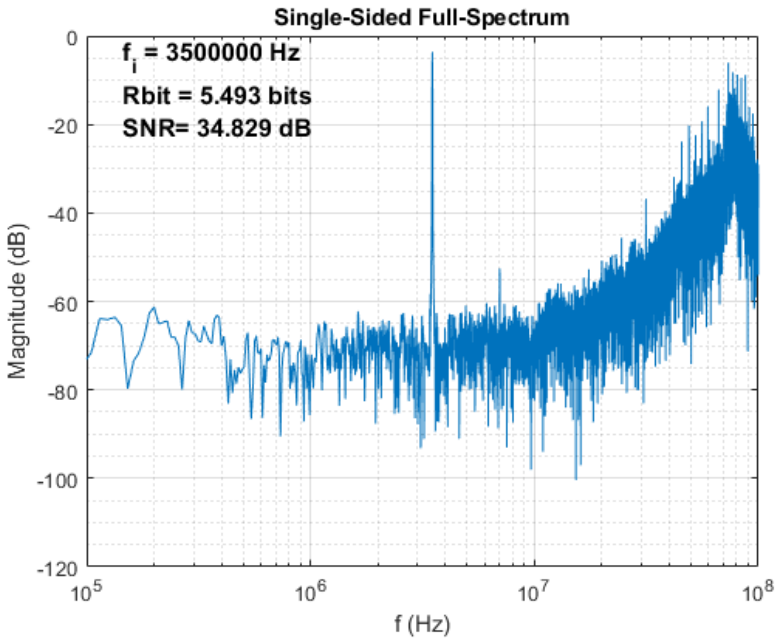


MEASUREMENTS

Full channel sinusoidal input







ENOB postlayout: 6.24 bits
ENOB measured: 5.493 bits

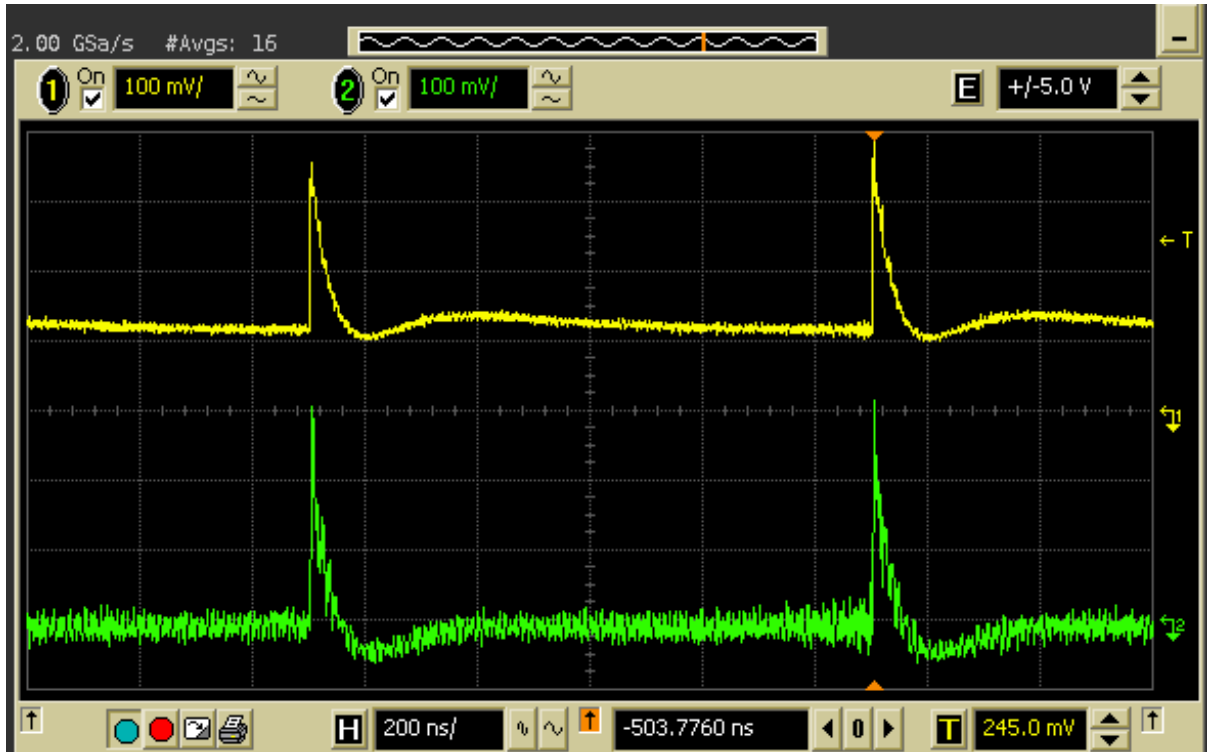
BW = 10 MHz
Fs = 1 GHz
OSR = 50

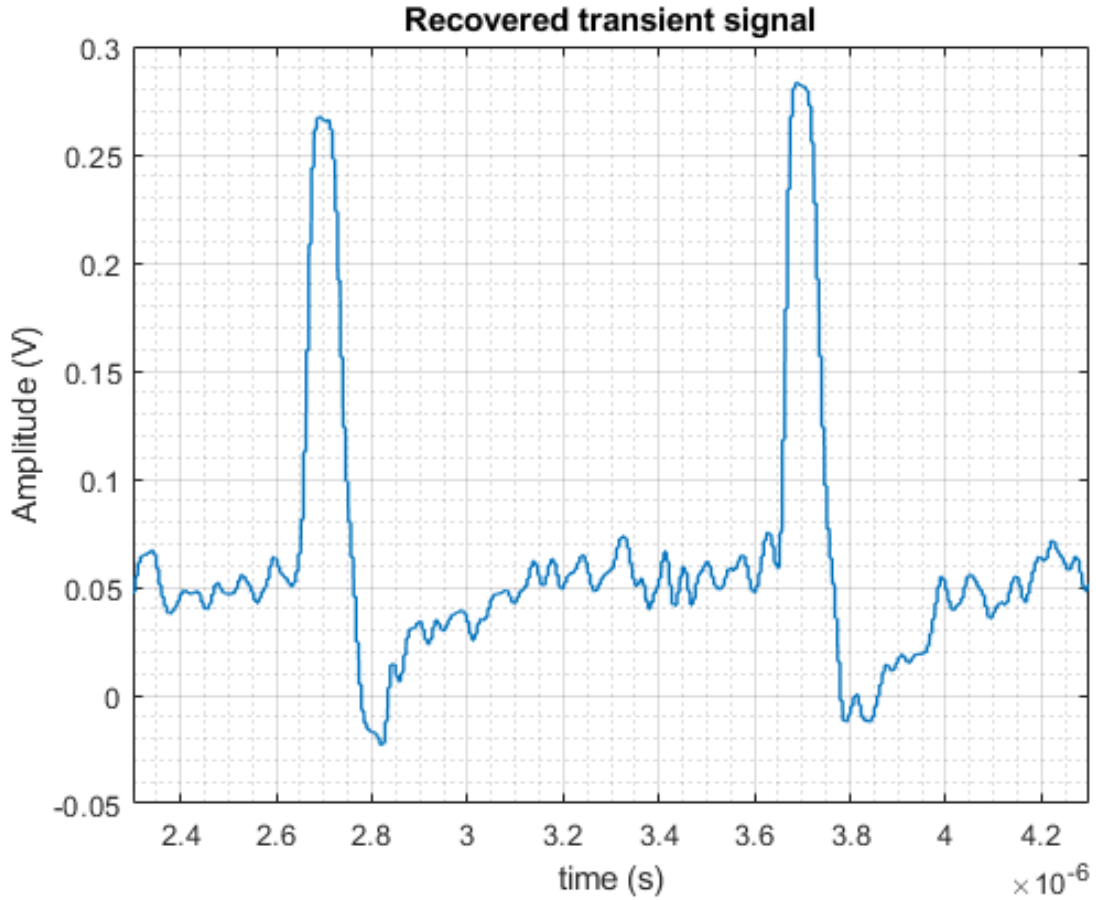
0.747 bits are lost due to:

- **Decoupling in sigma-delta transmission lines.**
- **HF cables must be changed to RF-10GHZ cables.**
- **Very-high noise in the laboratory .**

MEASUREMENTS

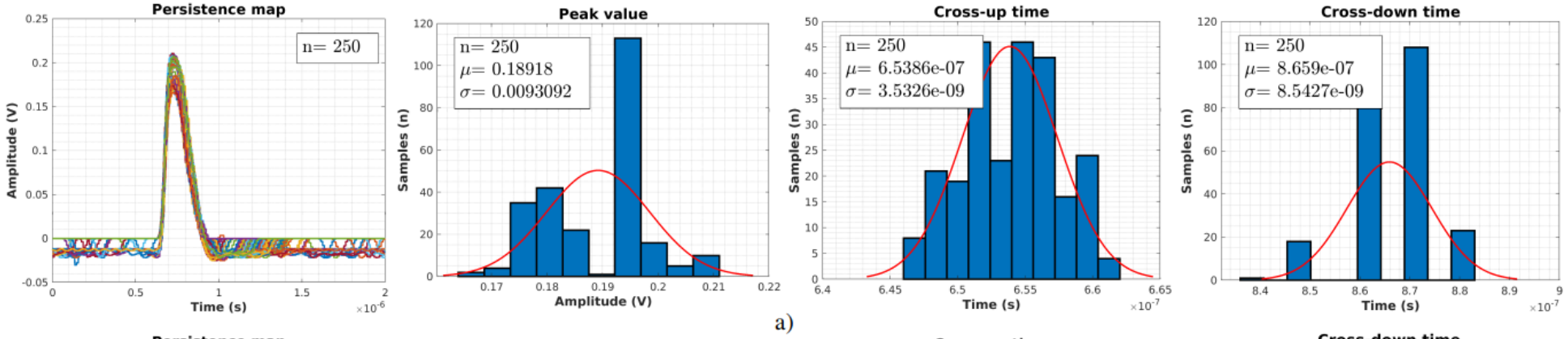
Full channel with SiPM





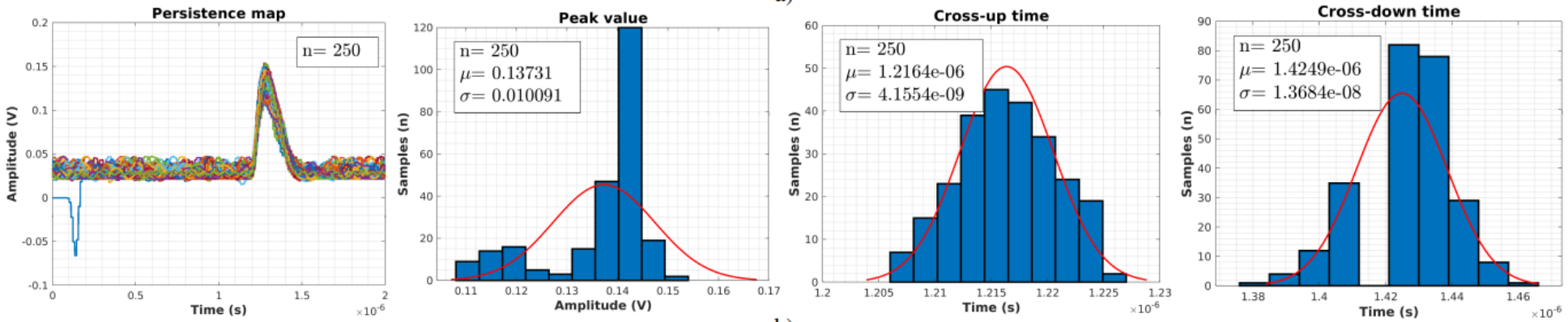
A 500 kHz SiPM signal is sucesfully recovered!!!

PERSISTENCE MEASUREMENTS. Low gain.



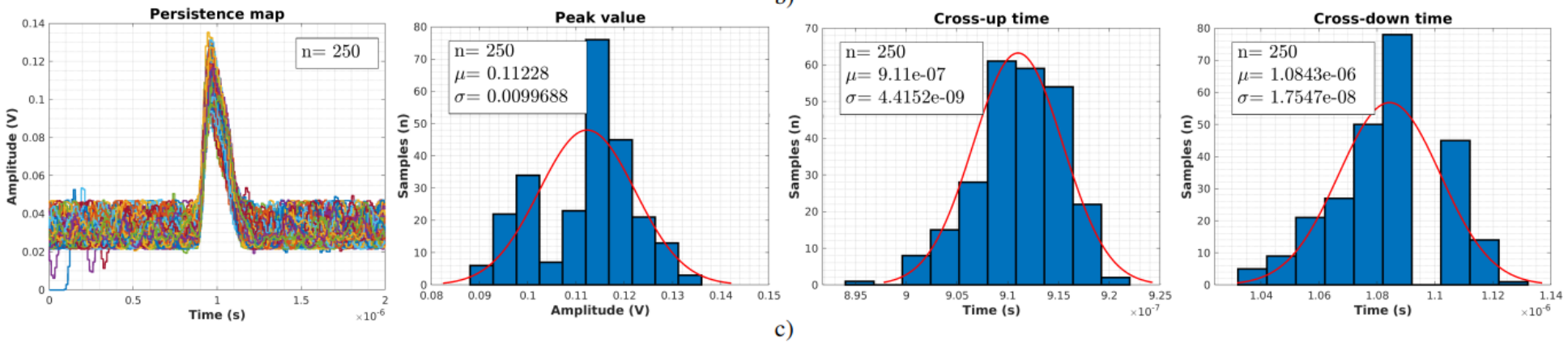
a)

Laser attenuation=70%
Vth=25mV



b)

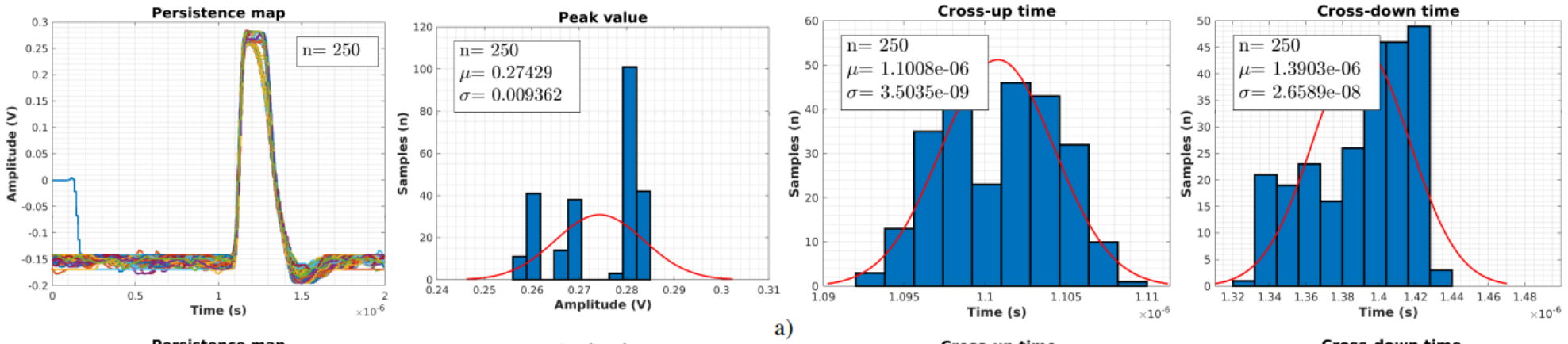
Laser attenuation=80%
Vth=60mV



c)

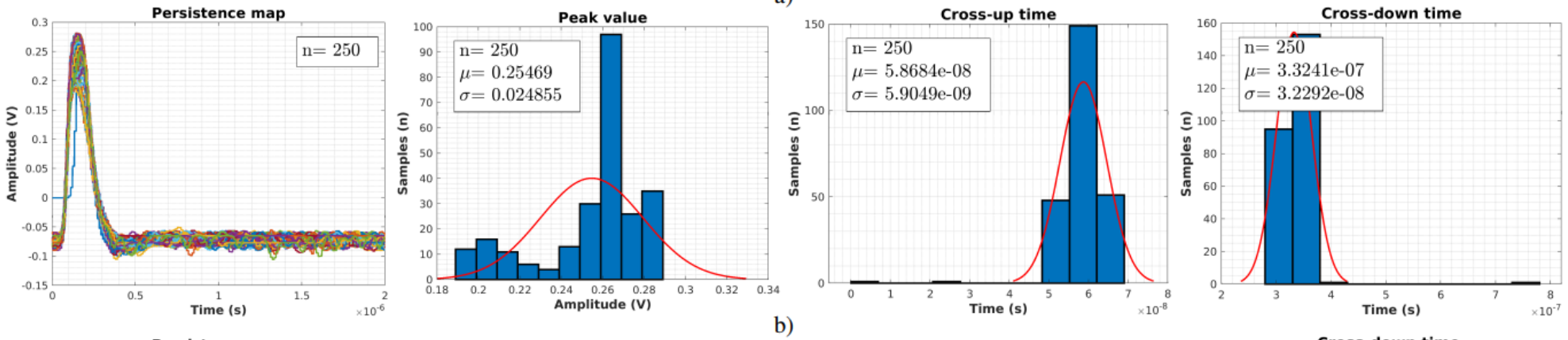
Laser attenuation=90%
Vth=65mV

PERSISTENCE MEASUREMENTS. High gain.



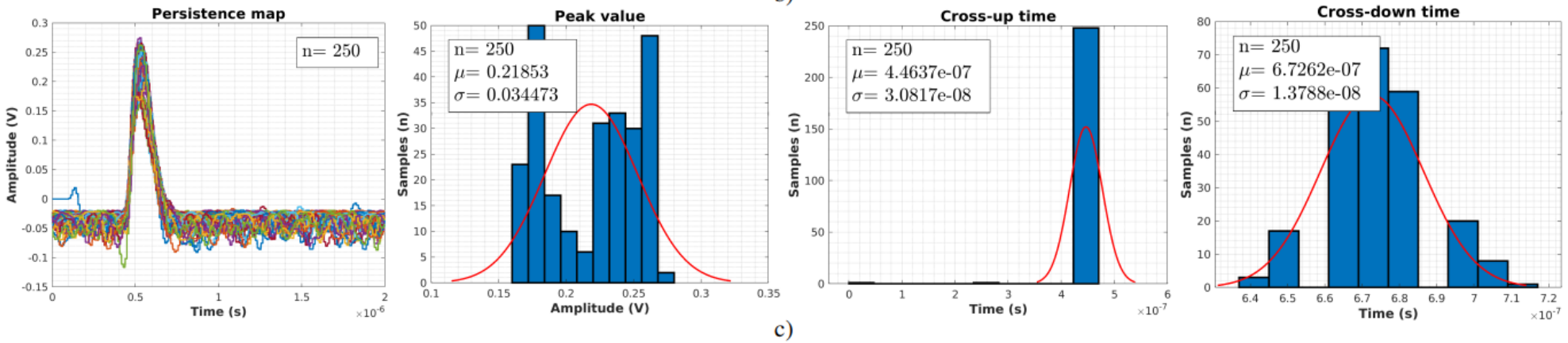
a)

Laser attenuation=70%
Vth=-100mV



b)

Laser attenuation=80%
Vth=-50mV



c)

Laser attenuation=90%
Vth=0 V

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Conclusions

- The MexSIC data adquisition channel for SiPMs was proposed, modeled and experimentally validated.
- The MexSIC is composed of a mixed-mode ASIC frontend and a FPGA-based processing stage.
- The proposed ASIC was capable of modulating, in the sigma-delta domain, a 0.1-1 mA SiPM current with a resolution of 5.493 bits and a bandwidth of 10 MHz.
- This bandwidth offers an information loss of only 1% for signals whose shape and time of flight lies on SiPMs.
- To complete the digitization of the SiPM signal, the FPGA performs a decimation process by means of a cascaded integrator filter.
- The ASIC was designed in a 180 nm CMOS standard process using Cadence© software and the processing stage was implemented in a Kintex-7 FPGA.

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THANK YOU!

Any questions?